Numerical Simulation of the Temperature on the Metallization of an Integrated Circuit and its Impact on Interconnect Lifetime

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Abstract—This paper uses a finite element model to investigate the temperature change of the interconnects of an integrated circuit due to the power dissipation of the transistors in the substrate. The temperature of the local interconnect is more significantly affected, exhibiting an increase of 49 K and 34 K, for the Metal 1 and Metal 2, respectively. We discuss the impact of the temperature increase in the electromigration and, as a consequence in the lifetime of the operational amplifier, which demonstrates the importance of considering the metallization temperature distribution in the design stage.

Index Terms—BEOL, reliability, electromigration, integrated circuit

I. INTRODUCTION

An accurate analysis of the temperature distribution on the interconnect structures is essential to a better understanding of the integrated circuit (IC) reliability. This can be accomplished, for example, by estimating the temperature of each layer of the back-end-of-line (BEOL) [1]. The temperature estimation becomes more relevant for the new technologies, which have a reduced distance between metal layers and transistors, being the BEOL more affected by temperature change due to the self-heating from transistors [2,3].

As the metal layers serve as a thermal path to the heat generated by the transistors, the temperature of the interconnect lines increases. The number of vias, the metal density, the metal thickness and the material contribute to a non-uniform temperature distribution [4-6]. Such a temperature distribution is of great importance to the IC designer and has to be considered for the performance and reliability evaluation at circuit level [7,8].

Under electromigration (EM), the wire is affected by voids, which leads to an increased interconnect resistance or even open circuits [9]. The high temperature accelerates the void evolution [10,11] and leads to faster IC performance degradation, and as a consequence the circuit lifetime reduces. Therefore, the interconnects have to be sized considering the temperature increase to guarantee an adequate circuit operation for a longer period. In this paper we simulate the temperature on the interconnect layers of an integrated circuit using a finite element model (FEM) where the main heat source is positioned in the center or in the corner of the circuit. We compare the results with the temperature estimated with an analytical model. The impact of the temperature change on the mean time-to-failure (MTTF) of an operational amplifier designed in 45 nm technology is evaluated.

II. TEMPERATURE EFFECT ON MTTF

Under EM, the interconnect resistance increase degrades the performance of circuits. The \((\Delta R/R_0)_{\text{crit}}\) is the resistance ratio value that results in a circuit performance change out of an acceptable range. Then, the time to reach this critical value can be considered the time to circuit failure and expressed by

\[
MTTF = \frac{kLA_b T}{D(T) e^{|Z^*| \rho_0 (T)}} \int \left( \frac{\Delta R}{R_0} \right)_{\text{crit}} \cdot (1)
\]

where \(D(T)\) is the diffusion coefficient, \(Z^*\) is effective valence, \(\rho_0(T)\) is the resistivity, \(e\) is the elementary charge, \(k\) is the Boltzmann’s constant, \(T\) is the temperature, \(I\) is the electrical current, \(A_b\) is the cross-sectional area of the barrier layer and \(L\) is the length of the line.

The EM is very sensitive to the temperature. Temperature changes affect the diffusion coefficient and the resistivity of lines. The diffusion coefficient follows an Arrhenius relation with an exponential variation with \(T\) given by

\[
D(T) = D_0 \exp \left( - \frac{E_a}{kT} \right). (2)
\]

Here, \(D_0\) is a pre-exponential factor and \(E_a\) is the activation energy, both dependent on the diffusion mechanisms. The line resistivity, \(\rho\), calculated by

\[
\rho = \rho_0 \left[ 1 + \alpha (T - T_0) \right], (3)
\]

deals on the resistivity \(\rho_0\) in the reference temperature \(T_0\) and the temperature coefficient \(\alpha\) of the metal.

Depending on the accuracy of the parameters used to calculate the resistance change, some lines initially classified as critical can be an EM safe line.

A resistance increase of 10% is generally used as a failure criterion, since this variation in global wiring can produce timing errors [12]. Using this percentage increase as a failure criterion has some limitations. First, the actual damage that causes the failure is a function of the initial resistance of the line, which is affected by the temperature and the stress during the fabrication [13]. Second, as the maximum resistance change depends on the width of the line, the current density, and the bias of the transistors, the resistance ratio can assume values higher than 10%, and the circuit continues to operate correctly or, on the other hand, it can be lower than 10% and the circuit does not satisfy the minimum performance.
III. FEM MODEL STRUCTURE

The finite element method (FEM) is a useful tool to understand the effect of heat transfer from transistors in the silicon substrate. With FEM, we simulate the temperature change ($\Delta T_{PT}$) in the interconnects with the 2D physical model based on the GPDK 45 nm Bulk CMOS technology [14]. The BEOL has 11 layers of interconnects and 10 of vias, with 6% of volume fraction of the vias and 40% of volume fraction of the metal in each layer. Fig. 1 shows the schematic of the model structure with four metal layers, nonetheless we simulate the eleven layers. A very low thermal conductivity epoxy resin isolates gold bond wires which are connected to the packaging. The thermal conductivity of the materials, dimensions of the vias and the metal layers, etc. are described in Table I.

Table I. Parameters used in the BEOL model simulated in the COMSOL.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si thickness</td>
<td>20</td>
<td>µm</td>
</tr>
<tr>
<td>Chip’s width</td>
<td>800</td>
<td>µm</td>
</tr>
<tr>
<td>Contact’s thickness</td>
<td>150</td>
<td>nm</td>
</tr>
<tr>
<td>Via1 and Via2 thickness</td>
<td>150</td>
<td>nm</td>
</tr>
<tr>
<td>Via3 to Via9 thickness</td>
<td>180</td>
<td>nm</td>
</tr>
<tr>
<td>Via10 and Via11 thickness</td>
<td>1000</td>
<td>nm</td>
</tr>
<tr>
<td>Metal1 and Metal2 thickness</td>
<td>150</td>
<td>nm</td>
</tr>
<tr>
<td>Metal3 to Metal8 thickness</td>
<td>180</td>
<td>nm</td>
</tr>
<tr>
<td>Metal9 to Metal11 thickness</td>
<td>1000</td>
<td>nm</td>
</tr>
<tr>
<td>Volume fraction of metal</td>
<td>0.4</td>
<td>n.a.</td>
</tr>
<tr>
<td>Contact width</td>
<td>65</td>
<td>nm</td>
</tr>
<tr>
<td>Via12 width</td>
<td>65</td>
<td>nm</td>
</tr>
<tr>
<td>Via23 and Via34 width</td>
<td>70</td>
<td>nm</td>
</tr>
<tr>
<td>Via45 to Via67 width</td>
<td>140</td>
<td>nm</td>
</tr>
<tr>
<td>Via78 and Via89 width</td>
<td>400</td>
<td>nm</td>
</tr>
<tr>
<td>Via910 and Via1011 width</td>
<td>800</td>
<td>nm</td>
</tr>
<tr>
<td>Volume fraction of via</td>
<td>0.06</td>
<td>n.a.</td>
</tr>
<tr>
<td>Distance between vias</td>
<td>500</td>
<td>nm</td>
</tr>
<tr>
<td>Heat source thickness</td>
<td>60</td>
<td>nm</td>
</tr>
<tr>
<td>Heat source width</td>
<td>2000</td>
<td>nm</td>
</tr>
<tr>
<td>Bondwire width</td>
<td>2000</td>
<td>nm</td>
</tr>
<tr>
<td>Packaging thickness</td>
<td>100</td>
<td>nm</td>
</tr>
<tr>
<td>Passivation thickness</td>
<td>5</td>
<td>nm</td>
</tr>
<tr>
<td>Resin thickness</td>
<td>80</td>
<td>µm</td>
</tr>
<tr>
<td>Si - Thermal conductivity</td>
<td>130</td>
<td>W/(K-m)</td>
</tr>
<tr>
<td>Cu bulk - Thermal conductivity</td>
<td>400</td>
<td>W/(K-m)</td>
</tr>
<tr>
<td>Acrylic - Thermal conductivity</td>
<td>0.18</td>
<td>W/(K-m)</td>
</tr>
<tr>
<td>SiO2 - Thermal conductivity</td>
<td>1.4</td>
<td>W/(K-m)</td>
</tr>
</tbody>
</table>

IV. BEOL TEMPERATURE SIMULATION

Based on the FEM model, we investigate the temperature on the BEOL with the transistors’ power dissipation of 400 W/m. The reference temperature is 293 K. Two studies are carried out: a) first we investigate the $\Delta T_{PT}$ in the metal layers, b) we evaluate the mean-time-to-failure (MTTF) change with the temperature.

Fig. 2 illustrates a temperature distribution on a chip with a length from $x_1$ to $x_2$ and a width from $y_1$ to $y_2$. In the first case, we simulate the thermal distribution on the BEOL from $x_1 = 240$ µm to $x_2 = 560$ µm and $y = 200$ µm with the primary heat source in the center of the chip at $x = 400$ µm and $y = 200$ µm. Here, the primary heat source in the center of the chip produces heat that flows into the BEOL and changes the temperature of the lines. The transistors occupy a small region of 2 µm, equivalent to 0.25% of the width of the chip, resulting in a higher temperature in a narrow central region of the metal lines. In a typical integrated circuit, the transistors occupy a larger area, and as a consequence, the temperature distribution is more homogeneous along the lines.

The temperature in regions further away from the heat source, in particular at the corners A, B, C, and D, undergoes a lower change. Besides the power dissipated by the transistors, the temperature change in each metallic layer ($\Delta T_{PT}$) is a function of thermal conductivity of the several materials, the geometry of the layers, and the number of vias.

Fig. 3 shows the temperature of lines from Metal 1 to Metal 11 from $x = 240$ to 560 µm. The interconnects of the local layers near the primary heat source operate under the highest temperatures. As expected, the temperature near the corners A, B at $x = 240$ µm and C, D at $x = 560$ µm are significantly lower than in the center of the chip. The result considers the vias distributed at the end of the metallic layers, in a formation named quasi-manhattan structure [17]. The concentration of the vias near the heat source between the layers M2-M3, M4-M5, M6-M7, M8-M9 and M10-M11 results in the same $\Delta T_{PT}$ for the lines of these layers.

In a second case, the primary heat source is near one of the chip’s corners, shown in Fig. 4. With the primary heat source near the corner A, the highest $\Delta T_{PT}$ of 57 K is at $x = 280$ µm, $y = 150$ µm and a lower $\Delta T_{PT}$ at the other corners, as shown in Fig. 5. Observe that the primary heat source sized
In the third case, the center and regions near the corners have heat sources with the same power dissipation of 400 W/m, as illustrated in Fig. 6. Fig. 7 shows the temperature along the BEOL with the heat sources at the center at \( x = 400 \mu m, y = 200 \mu m \) and near the corners A and D, at \( x = 280 \mu m, y = 150 \mu m \) and at \( x = 520 \mu m, y = 150 \mu m \). The inclusion of more heat sources increasing the power dissipated in the FEOL increases the temperature on the BEOL as observed in the Metal 10 layer, which has the maximum temperature of 311 K, equivalent to \( \Delta T_{PT} \) of 11 K. 4 K higher than the case 2, and 3 K higher than the case 1. Note that the Metal 2 in the position 280 \( \mu m \) has a temperature of 334 K, 5 K higher than the Metal 2 positioned in 400 \( \mu m \), in the center of the chip, indicating the influence of the position of the vias in the thermal distribution of the chip.

Fig. 8 shows a comparison between the maximum temperature change on each metal layer estimated with [18] and simulated with the primary heat source at the center, at the corner and at the center and the corner (Fig. 3, 5 and 7). A large temperature difference between two consecutive layers is observed in the three curves. The results indicate that in Metal 1 the \( \Delta T_{PT} \) is near to the simulated temperature change in Fig. 3, 5 and 7. The small differences in \( \Delta T_{PT} \) has a relation with the different materials used in the simulation, while the temperature estimated considers the effective conductivity from the Si and Cu. The distribution of the vias and the heat source position affect the temperature, evidenced by the differences between the temperatures simulated in Figs. 3 and 5.
V. MTTF CHANGE WITH TEMPERATURE

To evaluate the impact of the $\Delta T_{PT}$ in $\Delta R/R_0$ and in the circuit lifetime, we simulate 176 paths from interconnects of an operational amplifier shown in Fig. 9. The length and the width of the paths vary from 2 $\mu$m to 123 $\mu$m and from 0.06 $\mu$m to 1.7 $\mu$m, respectively, as illustrated in the histograms from Figure 10(a) and Figure 10(b). Here, the length is the largest metal line of an interconnect containing the path. The lines are designed with 3 metal layers, where 6 paths are Metal 1, 33 paths are Metal 1 and 137 paths are Metal 2, as shown in Figure 10(c). The resistance of each path is given in Figure 10(d). The histograms in Figure 10(e) and Figure 10(f) indicate the current density through the lines in relation to the maximum current density of 2 mA/\mu m for static and DC simulations. Note that some paths have the current density ratio ($J/J_{max}$) higher than 1 and operate under a current density above the maximum indicated by the technology.

The average power dissipated per transistor is 75 $\mu$W, equivalent to a normalized power of 416 W/m, for the transistor’s pitch of 180 nm. Fig. 11 shows the $\Delta T_{PT}$ of 61 K, 48 K and 42 K for the Metal 1, Metal 2 and Metal 3 respectively. This results in a temperature of 361 K, 348 K, and 342 K, for a reference temperature of 300 K. The importance to estimate the temperature by layer is evident when observing the temperature in Metal 1, which is 19 K higher than the estimated temperature in the Metal 3 layer. Although the local layers have elevated temperature, ICs can support higher temperatures. A chip designed for an industrial application, for example, supports maximum temperatures of 398 K [19].
Failure due to EM, considering only the temperature. Layers indicate that the local interconnects are more prone to technology. The large differences of temperature in the metal network results due to the power dissipation from transistors using new technology and has to be considered for the performance of circuits. The temperature increase due to the Joule heating and current crowding on electromigration in mobile technology. App. Phys. (2017),1-4.


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**REFERENCES**


Fig. 12: (a) Time to the resistance of the lines increase 10% with a $\Delta T_{PT}$ variation from -3% to 3%. Similar analysis with the critical resistance of the lines of 40%.

-3 -2 -1 0 1 2 3
PT variation (%)
0
1
2
3
4
5
6
MTTF 10 (years)
(a)

-3 -2 -1 0 1 2 3
PT variation (%)
0
1
2
3
4
5
6
MTTF 40 (years)
-3 -2 -1 0 1 2 3
PT variation (%)
0
0.5
1
1.5
MTTF 10 (years)
(b)