Analysis of the Correlation Between NBTI Effect and the Surface Potential in Junctionless Nanowire Transistors

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Abstract— **This paper discusses the nature of degradation by NBTI effect in pMOS junctionless nanowire transistors when varying the density of interface traps. The data obtained in simulations are analyzed through the extracted hole density together with the surface potential and it is demonstrated how the quality of gate oxide affects the performance of such transistors, when the density of traps, the channel width, the doping concentration and the gate bias are varied.**

Index Terms— **Junctionless nanowire transistor; NBTI; density of interface traps; hole density; surface potential.**

I. Introduction

Junctionless Nanowire Transistors (JNTs) [1] are devices developed with SOI technology, which present same doping type and concentration in source, drain and channel regions (usually in the order of 10^{19} cm^{-3}) as shown in Figure 1. JNTs work differently from inversion mode devices. The difference in the work function between the gate material and the silicon layer is between 0.5 and 1.0 V, making this layer completely depleted when the gate is biased at zero bias (V_{GS} = 0 V) [2]. Thus, there are no free carriers for the formation of a conduction layer. When a voltage is applied to the gate (positive in the case of nMOS transistors and negative in the case of pMOS), the depletion layer will have its depth decreased and progressively, the depleted region will reduce, forming a neutral path close to the center of the channel layer. When V_{GS} is increased above (below) the flatband for a n-type (p-type) device, the silicon layer leaves the depletion regime, allowing conduction to begin close to the interface. So that, it is a characteristic of the JNT that the majority of the current flows through the center of the channel and a smaller part close to the silicon-gate dielectric interface, as shown in Figure 2, which exhibits the current density for some biasing condition, i.e. off-state, at threshold, above threshold and above flatband conditions.

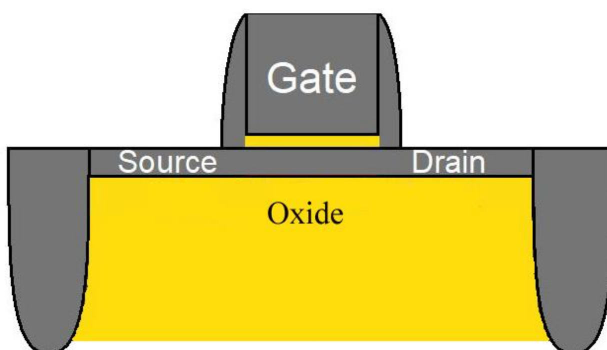

Fig.1 Longitudinal section of a Junctionless Nanowire Transistor.

This study focuses on the Negative Bias Temperature Instability (NBTI) effect [3] that originates from the fact that there are hydrogen atoms in the silicon-gate dielectric interface as shown in Figure 3. These atoms are inserted into the silicon along the fabrication process in order to passivate the interface, improving its quality. When the gate voltage is applied for a long period of time, the breakdown of hydrogen bonds with silicon doping atoms can occur [3]. In this case, free hydrogen atoms diffuse towards the interface, forming traps, which alter the threshold voltage (V_{TH}) of the device. The NBTI effect is observed in pMOS devices, as the diffusion of hydrogen from the substrate breaks the bonds of boron used as a dopant in pMOS transistors.

In inversion mode transistors, the surface potential can be assumed nearly constant when the device is biased in strong inversion, while the electric field varies almost linearly with the gate voltage. In the case of junctionless transistor, such relation depends on the operation regime of the

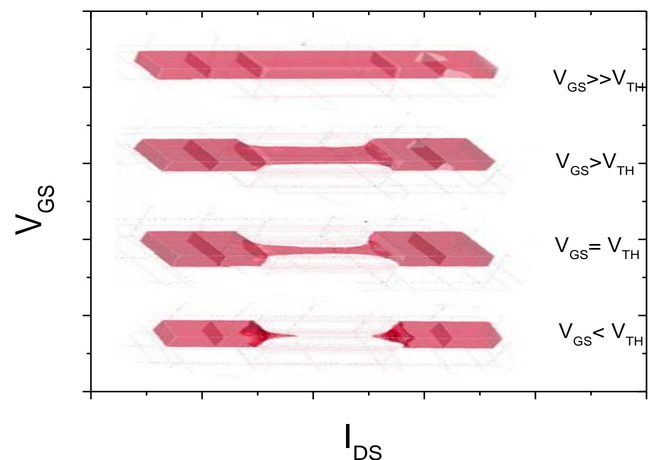

Fig.2 Behavior of the drain current as a function of the gate voltage.

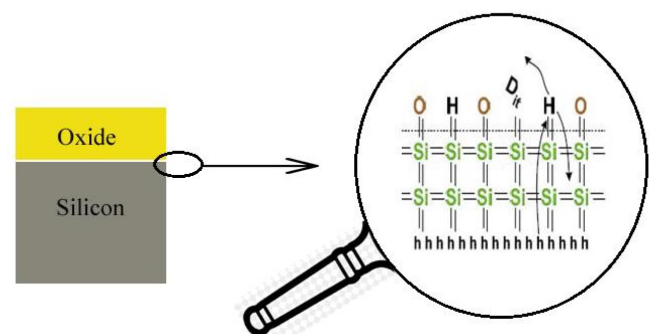

Fig.3 Hydrogen diffusion model

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device. Above flatband, when the device is biased in accumulation, the relationship between surface potential and the electric field is similar to the one observed in inversion mode transistors, i.e. the electric field is zero at flatband and its absolute values increases linearly with the absolute gate bias whereas the surface potential is nearly constant. However, junctionless devices were developed for working mainly in partial depletion regime. This condition is reached when the device is biased between the threshold voltage and the flatband. For gate voltage just above the threshold, a conduction path is formed far from surface, giving rise to a bulk conduction. In this case, the absolute electric filed reduces with the increase of the absolute gate voltage, till the devices reaches the flatband condition. So, the absolute maximum electric field in partial depletion occurs for a biasing condition in which the conduction layer is far from the surface where smaller NBTI incidence could be expected. Thus, as in such devices, a larger absolute electric field does not necessarily mean a stronger NBTI effect. Besides that, the electric field variation ratio with the gate bias is different in accumulation and partial depletion regimes. So that, the aim of this work is to perform the correlation between surface potential and NBTI, which, to the best of our knowledge has not been presented in previous works.

II. Characteristics of the Devices

To understand the physical phenomena that involve degradation by NBTI effect, 3D numerical simulations were performed using the Sentaurus tool [4]. The simulations have considered p-channel devices with different characteristics, such as, two doping concentrations, 5×10^{18} and 10^{19} cm^{-3}, and two different V_{DS} drain voltages, -50 mV and -1 V, as well as, two different fin widths W = 10 nm and 20 nm. The characteristics of the simulated devices are similar to the experimental ones described in [5] and their NBTI has been recently validated to the experimental ones in [6]. Such experiments results have shown similar trends with V_{GS} variation to the ones simulated. Also, when considering a precursor density (N_0) of $1x10^{12}$ cm^{-2} in the simulations, the absolute values for ΔV_{TH} resultant from NBTI are very close to the experimental ones obtained in [6]. So that, in the present work, the simulation setup has been considered identical to the one from [6]. For the simulation analysis, the density of precursor was varied between 5×10^{11} and 5×10^{13} cm^{-2}. The same precursor density was considered both at both top and lateral gates, without accounting for any differences in the quality of the interfaces due to fabrication process/crystallographic orientations. According to the experimental results from [6], such assumption has shown to be valid.

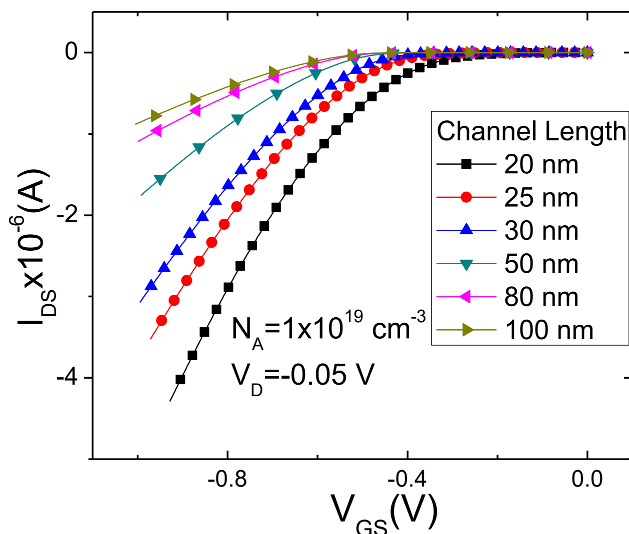

Fig.4 Drain current as a function of gate voltage for JNTs devices with 1×10^{19} cm^{-3} channel doping and V_{DS} = -0.05 V.

Models that represent the generation and recombination of the carriers, the dependence of mobility on longitudinal electric field and the narrowing of bandgap were considered in all simulations. The NBTI effect was simulated by applying a two-stage degradation model [7-8], in which the energy levels involved, and activation energies are widely distributed and are treated as random variables [4].

Among the calculated variables, we have the density of interface traps (Nit). If the interface between gate oxide and silicon is more subject to interface traps, it can be said that the NBTI effect will be more intense and, consequently, there will be a reduction in the drain current for the same gate voltage. Therefore, there will be a reduction of the threshold voltage. Figure 4 shows how the I_{DS} x V_{GS} curves behave for devices with different channel lengths without accounting for the NBTI effect. From Figure 4, it can be noted that the V_{TH} of the devices is reduced (in module) by reducing the channel length of the devices. This behavior is related to the influence of short channel effects. The extracted values of the threshold voltage as well as the flatband voltage for 40 nm-long devices with different doping concentrations and widths before stress are shown in Table 1.

Table 1 – Threshold voltage for simulated 40 nm-long devices with different channel doping concentrations and widths biased at V_{DS} = -0.05 V and -1.0V before gate voltage stress.

N_A (cm^{-3})	V_{FB} (V)	L (nm)	W (nm)	V_{TH} (V) (V_{DS}=-0.05 V)	V_{TH} (V) (V_{DS}=-1.0 V)
5×10^{18}	-1.05	40	10	-0.71	-0.50
			20	-0.49	-0.05
1×10^{19}	-1.06	40	10	-0.65	-0.43
			20	-0.36	0.08

III. Influence of Nit On NBTI Degradation

As already mentioned, the density of interface traps reflects the quality of the gate oxide. The lower this characteristic, better the manufacturing process. So that, the simulations have considered different densities of precursor, as well as gate voltage overdrives ($V_{GT} = V_{GS}–V_{TH}$). Figure 5 presents the threshold voltage variation due to the NBTI effect (ΔV_{TH}) as a function of N_0. For the ΔV_{TH} extraction, a transient simulation considering a gate voltage stress for an interval of 1000 seconds is performed, which results in the drain current reduction due to NBTI model. It is considered that the whole current reduction is related to the threshold voltage variation. By comparing the final drain current to the initial I_{DS} x V_{GS} curves as shown in Fig. 4, the threshold voltage variation is obtained.

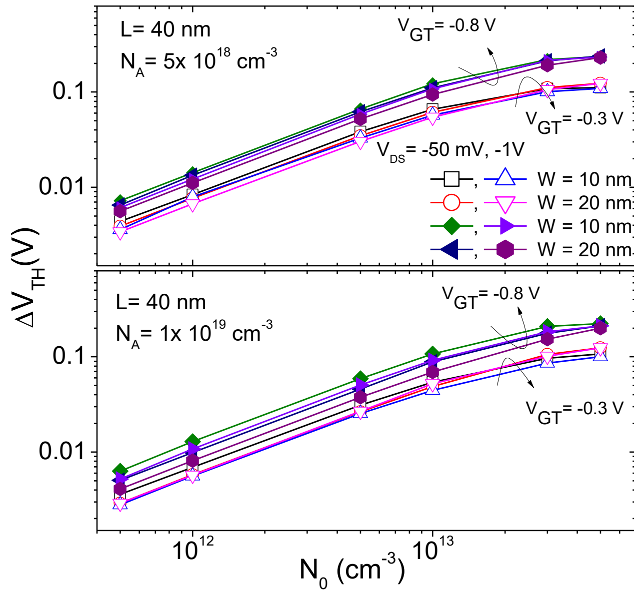

Fig.5 V_{TH} degradation by NBTI effect as a function of N_0 for devices with different doping concentrations, V_{GT} and W.

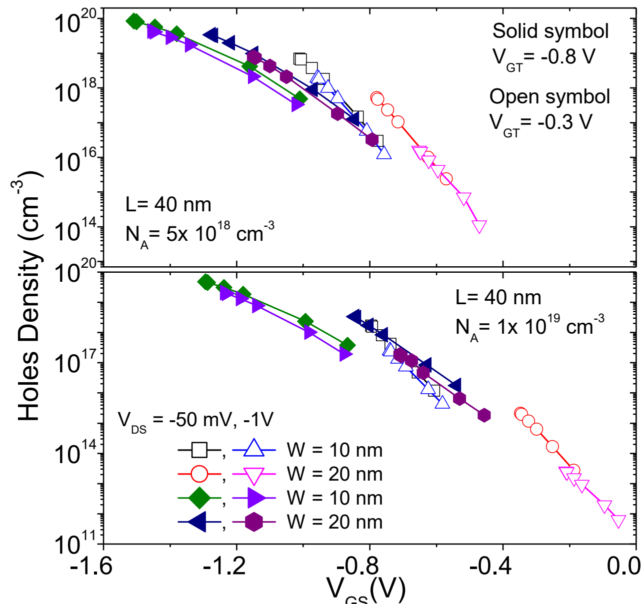

Fig.6 Density of holes as a function of the gate voltage for devices with different W, N_A and bias condition.

It can be seen, in Figure 5, that the NBTI effect is intensified with an increase in the density of precursor and N_0 higher than 2×10^{13} cm^{-3}, the tendency of the curves is to reach a nearly constant value. This can be explained by the fact that the adopted N_0 represents the maximum limit for the interface trap density of the model applied in the simulations, as shown in expression (1) [7]:

$$N_{it,SP}(r,t,E_{SP}) = P_{SP}N_0[1-e^{-K_{SP}(r,E_{SP})t}] \quad (1)$$

where P_{SP} is the probability of generating defects by the single particle interface intercept density processes (SP); E_{SP} is the activation energy for SP processes and K_{SP} (r, E_{SP}) is the reaction rate for SP processes.

As hydrogen ions are limited, the increase in the number of N_0 interface traps, tends to decrease P_{SP} and the resulting N_{IT}, tends to stability [4]. It is also evident when observing Figure 5 that, for drain voltage of -50 mV, for the smaller channel width (W = 10 nm) and for V_{GT} = -0.8 V, the effect NBTI is more significant. It is possible to conclude, when comparing the results obtained with N_A of 5×10^{18} cm^{-3} and with 1×10^{19} cm^{-3} that, for the lower doping, there is a greater degradation by NBTI effect, because, for these conditions, the V_{GS} biasing is greater or closer to the flatband at the same V_{GT}, since these devices present larger $|V_{TH}|$.

As demonstrated, the increment in N_0 density results in the increase of the NBTI effect. To better analyze the NBTI influence, the density of holes was extracted at the interface silicon/gate dielectric at the center of the top gate. The extracted hole density is presented in Fig. 6 as a function of the gate voltage for devices with different width and doping concentration, considering gate overdrive voltages of -0.3 and -0.8 V. It is worth mentioning that, when N_0 is increased, the trap density also increases, affecting the threshold voltage due to the NBTI. Therefore, when a device is considered at a fixed operating condition, i.e. fixed gate overdrive voltage, an increase in N_0 results in a decrease of $|V_{GS}|$, to compensate the threshold voltage variation.

Holes densities smaller than the doping concentration of the channel region indicates that the surface of the device is not conducting, i.e. there is no accumulation layer formed, but the device is conducting through the body, operating in partial depletion.

For the device with smaller channel width (W = 10 nm) and $N_A = 5 \times 10^{18}$ cm^{-3} at V_{GT} = -0.8 V, the holes density is higher as it can be seen in Figure 6(top). The greater the V_{GS} bias, the higher the density of holes, indicating that the device is operating deeper in the accumulation regime. Devices with a higher N_0 present a higher V_{TH} and, therefore, are biased deeper in the accumulation in the same V_{GT}, which results in a higher density of holes.

IV. Influence of Φ_S on NBTI Degradation

The JNTs also differ from the inversion mode devices with respect to the surface potential (Φ_S). For inversion mode devices, the Φ_S tends to remain constant with a value close to $2\Phi_F$ (where Φ_F is the Fermi potential), when the device is in the on-state condition [9]. For JNTs devices, since the Φ_S is zero at the flatband condition, it can have both positive and negative values depending if the device is in accumulation regime or partial depletion condition [10,11]. To analyze the relation between the surface potential and the NBTI effect, Φ_S was extracted at the middle of the top gate close to the gate dielectric/silicon interface. It is important to mention that in Junctionless devices, most of the current flows through the center of the channel. However, as the NBTI effect is related to traps generated at the gate dielectric/silicon interface, the potential was extracted at the surface.

In Figure 7, the extracted surface potential is presented as a function of the gate voltage for devices with different width, doping concentration and N_0. It is worth mentioning that the simulator uses the intrinsic Fermi level of silicon as

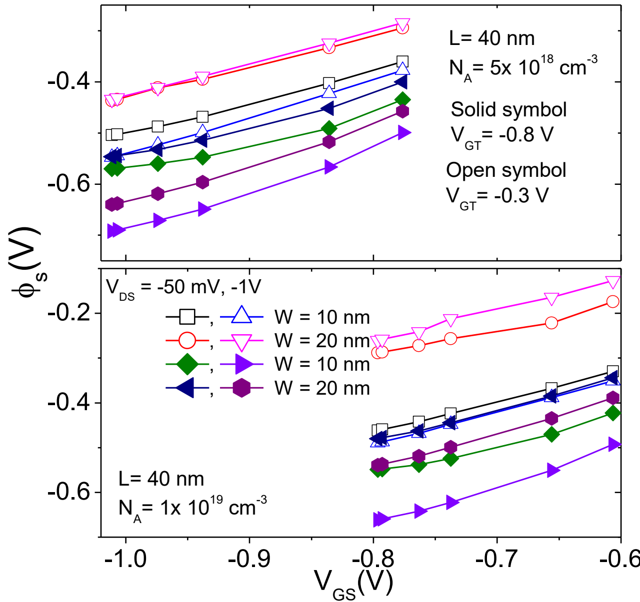

Fig.7 Φ_S as a function of the gate voltage for devices with different W, N_A and N_0.

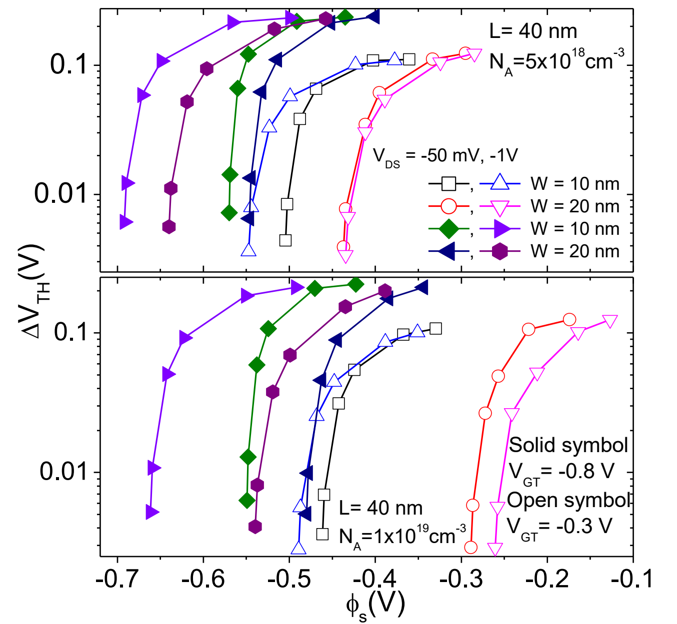

Fig.9 ΔV_{TH} as a function of the Φ_S for devices with different W, doping concentrations and N_0.

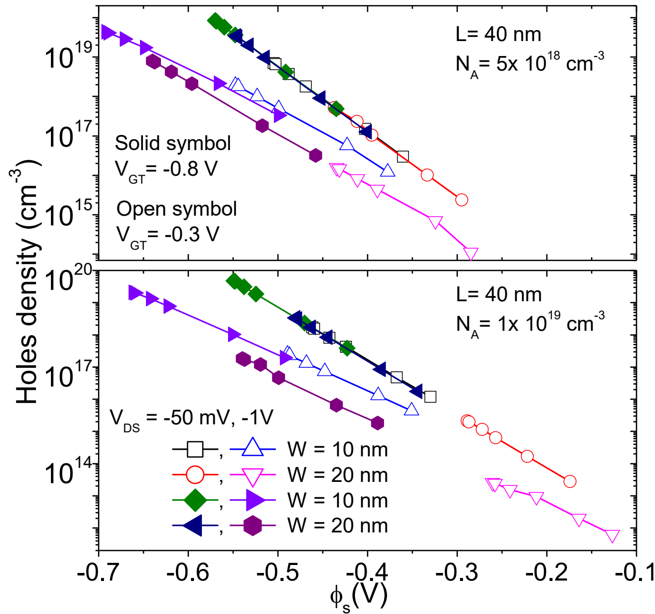

Fig.8 Density of holes as a function of the Φ_S for devices with different W, N_A and N_0.

reference. So that, a surface potential of $-\Phi_F$, represents the flatband condition. It should also be pointed that, as the potential was extracted at the middle of the channel, the quasi-Fermi level is also shifted by the channel potential induced by the drain bias. It can be observed that, for lower gate voltages, the surface potential is lower than $-\Phi_F$, indicating that the devices are in accumulation layer condition. As V_{GS} is increased, $|\Phi_S|$ decreases, as long as the devices are operating in the partial depletion condition. With the highest $|V_{GT}|$ (-0,8 V), a condition that biases the device further inside the accumulation, the V_{DS} of -1 V and W = 10 nm has the highest values of $|\Phi_S|$ for the same V_{GS}. These are also the same parameters for the largest NBTI, since, in this condition, the electric field is higher at the gate dielectric.

On the other hand, Figure 8 aims to show the relationship between Φ_S and the density of holes at the surface. In this case, the rise of $|\Phi_S|$ increases the density of holes. For V_{GT} = -0.8 V, W = 10 nm and V_{DS} = -50 mV, the highest values for the density of holes are found.

In Figure 9, the threshold voltage variation due to NBTI is presented as a function of the surface potential. It is possible to observe that the highest values of ΔV_{TH} occur for lower values of $|\Phi_S|$, demonstrating that for higher NBTI influence, the absolute value of the surface potential is reduced. Thus, the device leaves the accumulation regime conduction, entering in the partial depletion condition. Besides, higher $|V_{GT}|$ values (-0.8 V) and lower $|V_{DS}|$ values (-50 mV) imply a higher ΔV_{TH}, since this condition represents a stronger electric field at the gate. Wider devices are operating at the partial depletion condition according for any evaluated V_{GS}. So, to the extracted surface potentials and hole density, such devices always present a lower NBTI effect.

V. Conclusions

This work has presented an analysis of the Negative Bias Temperature Instability in p-type Junctionless Nanowire Transistors focusing on the hole density and surface potential behaviors. It can be observed that, when the precursor density is higher, the formation of trap increases, leading to a higher threshold voltage degradation, which reduces the surface potential, such that the device leaves the accumulation regime towards the partial depletion. Wider devices, which operates deeper in the partial depletion, seems to present lower NBTI degradation.

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