Digital Circuits and Systems based on Single-Electron Tunneling Technology

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***Abstract*— In this work, digital circuits and systems based on single-electron tunneling technology will be presented and analyzed. A simple design methodology will be proposed using a programmable single-electron NAND/NOR gate as a building block. Aspects such as operating temperature, noise, and charge fluctuations will be discussed. SET devices can reach ultra-low power consumption and high frequencies during operation. Although there are already many digital SET circuits and systems previously proposed and studied, there are few works about design methodology for SETs. This study shows a proposal for designing combinational and sequential single-electron circuits aiming at systems design. In the end, this work reinforces the use of single-electron technology as a possible large scale device in the future.**

***Index Terms*— single-electron tunneling; single-electron transistor; digital design; room temperature.**

I. Introduction

In the last 50 years, the advance of electronics has been based on shrinking the characteristic dimensions of MOS transistors. This evolution has led to the feasibility of nanoscale dimensions and opened up studies about new computational paradigms and design based on emerging technologies such as nanodevices. Among nanodevices, single-electron transistor (SET) - based on single-electron tunneling technology - emerges as a promising device for developing hardware[1, 2]. Moreover, there are many studies about how to fabricate and how to make circuits with SETs, and results show that SET has a huge potential for designing ultra-large-scale circuits in the future.

Single-electron transistors present attractive features such as extremely low power consumption, reduced dimensions, excellent current control, and low noise behavior. However, single-electron devices are quite sensitive to environmental conditions and their behavior is strongly dependent on temperature, as well as on offset charges and co-tunneling events [3, 1, 2, 4, 5]. To minimize or to overcome these issues [6], some measures were taken into account in this study.

Several different circuits based on single-electron tunneling technology have already been proposed for various analog and digital applications. Most of those circuits were designed to work under room temperature and at very strict voltage/current input values. Up to now, there is still no well-established design methodology.

In this work SET digital circuits and systems will be proposed. SET basics and the building block of the design methodology will be shown. Environmental conditions, such as temperature and offset charges, will be taken into account. Some combinational and sequential examples will be presented and validated by simulation. Finally, two digital systems previously implemented with this design methodology will be presented: a static random access memory (SRAM) and an astrocyte system.

II. Single-electron tunneling technology

In single-electron tunneling technology, in addition to smaller dimensions, a quantum mechanical phenomenon is responsible for the predominant charge transport mechanism: tunneling [3, 1, 2, 4, 5]. Typically, single-electron circuits are based on tunnel junctions, across which the charge flow is discrete. A tunnel junction is composed by an ultra-thin insulator barrier between two conductor materials as shown in Fig. 1. It can be modeled by two electrical parameters, a tunnel resistance (R_T) and a junction capacitance (C_J).

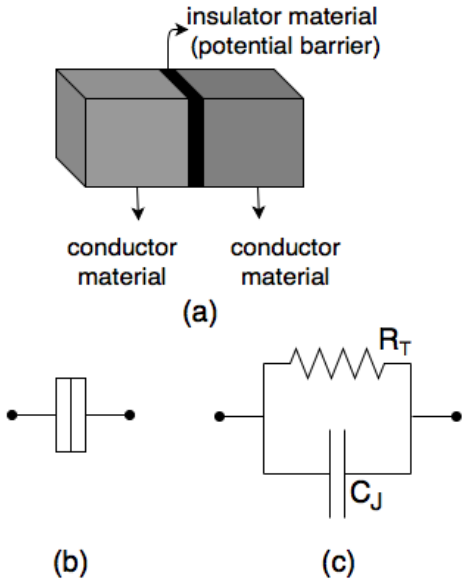

Fig. 1: Tunnel junction: (a) physical structure, (b) symbol and (c) electric model.

To guarantee the tunneling effect, the barrier thickness must be around $1nm$ or smaller. Building devices with such a small dimension aiming at large scale integration is a great challenge. In this sense, it is expected that new materials, such as graphene, would replace silicon in the future due to its functional limitations when it comes to shrinkage [7].

A. Single-Electron Transistor

The single-electron transistor has two tunnel junctions connected, forming a region called island between them, as shown in Fig. 2 [3, 1, 2, 4]. Hence, the voltage drop between V_D and V_S provides enough energy for the electron

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to tunnel through the barriers. On the other hand, the gate voltage (V_G) regulates the Fermi level, i.e., the highest energy level occupied on the island, therefore controlling the charge flow across the transistor [8]. It is worth mentioning that the smaller the dimension of the island, the higher the temperature the SET can operate at. Despite the fabrication challenge of such small devices, the operation of SETs up to 350 K has already been reported [4, 9, 10, 11].

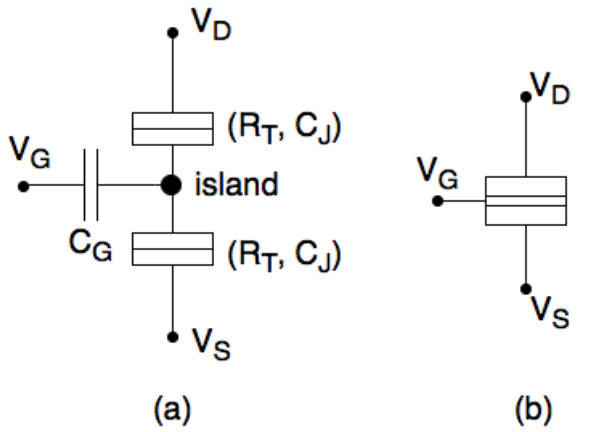

Fig. 2 Single-electron transistor: (a)transistor schematic and (b) symbol.

To achieve room temperature operation, two critical points must be observed:

- the charging energy (E_C) in the island should be greater than the thermal energy (E_T). So, according to it:

$$E_C >> E_T \tag{1}$$

$$\frac{e^2}{2C_{eq}} >> k_B.T \tag{2}$$

where e is the elementary electron charge, k_B is the Boltzmann constant, T is the operating temperature and C_{eq} is the total capacitance around the island:

$$C_{eq} = 2C_J + C_G \tag{3}$$

where C_J is the junction capacitance and C_G is the gate capacitance. The above restriction guarantee tunneling as the major charge transport mechanism;

- the total charge in the island is related to the equivalent capacitance of this node multiplied by the applied voltage:

$$Q = C_G.V_G \tag{4}$$

For obtaining single-electron transport, usually $Q = e$ where e is the electron elementary charge.

Fig. 3 proposes a flowchart with the steps for designing a SET based on the operating temperature and the applied voltage.

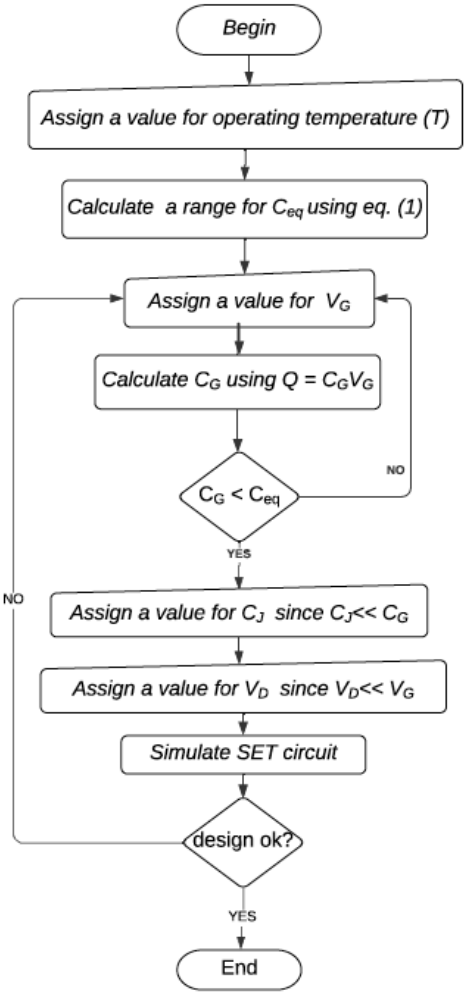

Fig. 3 Single-electron transistor design flowchart.

III. SET NAND/NOR PROGRAMMABLE LOGIC GATE

In the literature, some SET logic gates have already been proposed [12, 13, 14, 15, 16, 17, 2, 18, 19, 20, 21]. In particular, different circuit architectures of SET-NANDs can be found in [2, 18, 19]. The programmable single-electron NAND/NOR gate showed by Gerousis *et al.* [2] was later on deeply analyzed by Tsiolakis *et al.*[22]. This specific SET programmable gate showed stability and energy efficiency, which are interesting parameters for large scale circuits. Furthermore, the same SET gate was used to implement many digital circuits, showing no serious connectivity issues [23, 24, 25].

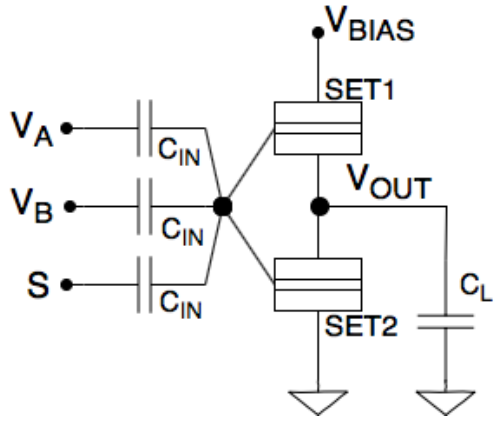

Fig. 4 SET programmable NAND/NOR gate.

In Fig. 4 voltages V_A and V_B are the inputs A and B, respectively. Voltage S is a select input that enables either the NOR function on the output of the gate when its value is high or the NAND function when its value is low. Both NAND and NOR Boolean functions have the property of functional completeness, i.e., any Boolean expression can be rewritten using only NAND or only NOR operations. Based on this property, all circuits in this work were implemented based on NAND gates.

To design the SET-NAND gate for room temperature operation, both SETs in the circuit (Fig. 4) were considered equal ($SET1 = SET2$). It is worth mentioning that, the flowchart in Fig.3 was adopted considering $V_D = V_{BIAS}$ and $V_G = V_{HIGH}$, where V_{HIGH} is the high-level voltage. Hence, the only values other than the transistors left to design are capacitances C_{in} and C_L. Empirically, it was determined that C_{in} should be chosen between 10 to 20 times greater than the C_G, while C_L must be approximately in the same order of C_G. The circuit parameters for the designed SET-NAND are shown in Table I.

In the following sections, all proposed digital circuits and systems were designed using the SET programmable gate presented in Fig. 4 as a building block. All simulations were executed using the LTSpice software [26] and using a SPICE model for the single-electron transistor proposed by Lientsching *et al.* [27]. Before connecting the transistors to form combinational and sequential circuits, a preliminary analysis of noise margins will be shown. Besides that, the performance of the SET-NAND gate including offset charges will be also studied.

Table I. SET-NAND gate circuit values

circuit parameter	value
C_j	0.01 aF
R_T	1 MΩ
C_g	0.15 aF
C_{in}	2 aF
C_L	0.2 aF
V_{bias}	0.5 V
V_A	0 V (low) and 0.5 V (high)
V_B	0 V (low) and 0.5 V (high)
S	0 V

A. *Noise margin analysis*

As already stated, the SET-NAND gate configured from Fig. 4 under analysis is used as the basic structure of all other circuits that will be presented in this work. Thus, the logic levels of all the following circuits will be determined by the operation of that gate. For this reason, it is interesting to analyze its noise margin, which is a quantitative measure of noise immunity of a logic circuit. A preliminary analysis of noise margin based on concepts used for CMOS technology was carried out by Telles *et al.* [24]. This analysis was performed by connecting the SET-NAND as an INVERTER just by making the two inputs ($A = B = V_{in}$) equal and obtaining the DC output voltage characteristic (V_{out}). The voltage transfer characteristic $Vout$ as a function of V_{in} was simulated at 300 K as shown in Fig. 5.

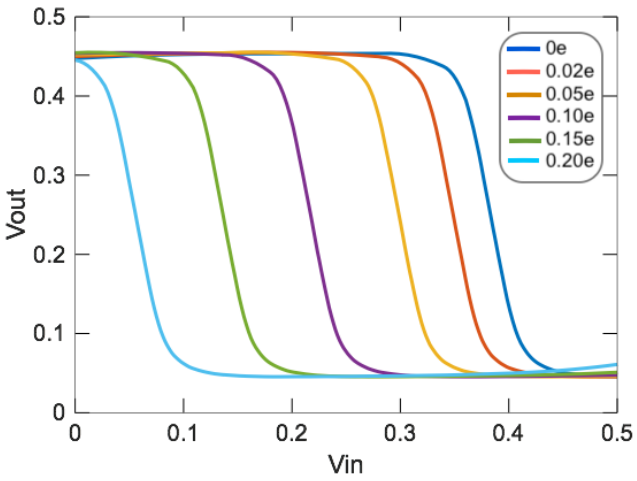

Fig. 5: SET-NAND/NOR voltage transfer characteristic considering different levels of offset charges in the following ranges: 0 (no background charges - ideal), between $-0.02e$ and $0.02e$ (2% of e), between $-0.05e$ and $0.05e$ (5% of e), between $-0.1e$ and $0.1e$ (10% of e), between $-0.15e$ and $0.15e$ (15% of e) and between $-0.2e$, and $0.2e$ (20% of e).

Also, a background charge robustness analysis was obtained by including random offset charges in the SETs' islands during simulations. Background charges are impurities introduced into the circuit, mainly by the manufacturing process. These charges can influence the SET operation, which in principle operates by transporting discrete quantities of electrons. It is important to note that studies predict that, in an optimistic estimate, 1 in every 1000 SET circuits will have

considerable fluctuations due to the background charges [1]. So, offset charges, varying from 0% to 20% of the elementary electron charge, i.e., in the range from $(-0.2e)$ to $(0.2e)$, were randomly introduced during the simulation. In this analysis, the device temperature was kept constant at $300K$.

Therefore, from Fig. 5 it is possible to calculate low-level noise margin (NM_L) and high-level logic margin (NM_H) for each simulation environment, i.e., from no offset charges to 20% of offset charges randomly spread over the SET-NAND circuit. For estimating the noise margin, the parameters obtained from each voltage transfer characteristic were:

- V_{IL}, the maximum input voltage that will be recognized as a low input logic level;
- V_{IH}, the maximum input voltage that will be recognized as a high input logic level;
- V_{OH}, the output voltage corresponding to an input voltage of V_{IL}; and
- V_{OL}, the output voltage corresponding to an input voltage of V_{IH}.

Generally, it is reasonable to maximize noise margins for better noise immunity. The values presented in Table II are relatively higher than the values provided by the CMOS technology, which seems an interesting advantage, considering that SET circuits are prone to local fluctuations and, consequently, to small changes in voltage values [1, 5, 28].

As can be seen, including random background charge effect shifts the high/low-level transition of the device to the left. As shown in Fig. 5, up to 10% of random charges is not only tolerable but also beneficial for the device since it brings the noise margin closer to ideal values [28]. It can also be stated that the SET-NAND gate is more robust against random background charges, which happens because its architecture is original, i.e., it is not a copy of the CMOS-based NAND gate architecture [28, 29].

IV. Combinational Circuits

To implement digital circuits with the SET-NAND presented in the previous section, all logic gates have been transformed into NAND gates, using the property of functional completeness already mentioned. For example, in Fig. 6 the circuit of a 2×1 MUX is implemented using NAND gates only.

The same circuit in Fig. 6 can be implemented in SET technology just replacing each NAND by the SET-NAND gate. The complete circuit is shown in Fig. 7. Just to exemplify the design of combinational circuits based on NAND gates presented here, the SET-MUX circuit was simulated using arbitrary inputs. Results are presented in Fig. 8. It is worth mentioning that the SET-MUX circuit was simulated at room temperature and including random offset charges effect in the range between $-0.05e$ and $0.05e$.

V. Sequential Circuits

Sequential circuits are made up of latches or flip-flops and combinational gates. Many single-electron flip-flops have

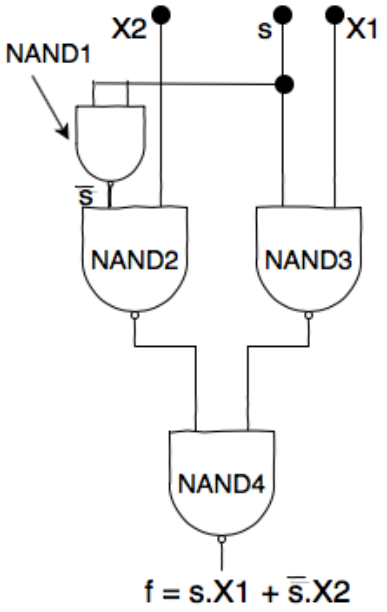

Fig. 6 MUX circuit based on NAND gates.

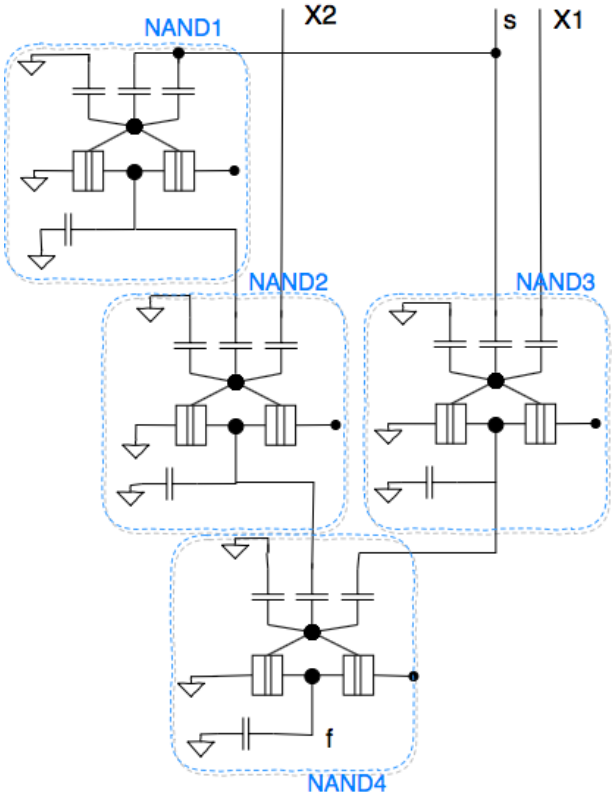

Fig. 7 SET-MUX circuit.

Table II. Noise margin values for different random offset charges.

Parameter	Random offset charges					
	0%	2%	5%	10%	15%	20%
V_{IL}	0.340	0.320	0.256	0.179	0.105	0.023
V_{IH}	0.411	0.375	0.327	0.248	0.170	0.081
V_{OL}	0.088	0.091	0.086	0.082	0.075	0.096
V_{OH}	0.437	0.415	0.436	0.430	0.419	0.421
NM_H	0.026	0.040	0.109	0.182	0.249	0.340
. NM_L	0.252	0.229	0.170	0.097	0.030	-0.073

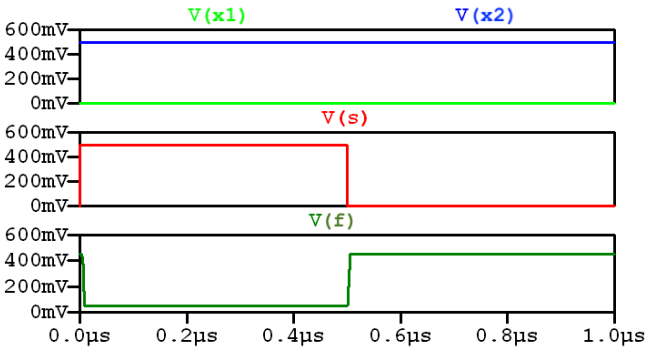

Fig. 8: Simulation results at room temperature for the SET-MUX using arbitrary input signals.

already been proposed. Hadley *et al.* [30] proposed different RS flip-flops. Yano *et al.* [31] presented a single-electron memory in which information can be read and written using SET-MOS devices. Besides, Wasshuber *et al.* [32] gave some examples of memory cells which can be individually used for simple storage and Lageweg *et al.* [33] proposed single-electron latches and flip-flops based on threshold gates. Moreover, Pradhan *et al.* [34] designed SR, D, and T flip-flops based on AND, INVERTER, and NOR gates. Nevertheless, none of these proposals were directly designed for applications at room temperature operation. Telles *et al.* proposed a D flip-flop based on the design technology presented in this work. The whole circuit, based on SETs, is shown in Fig. 9.

Simulation results for the SET D flip-flop using arbitrary inputs are presented in Fig. 10. Like the SET-MUX, it is worth mentioning that the SET d flip-flop circuit was simulated at room temperature and including random offset charges effect in the range between $-0.05e$ and $0.05e$.

VI. Digital Systems

As shown in the previous sections, it is possible to successfully implement combinational and sequential circuits using a SET-NAND gate as a building block. Therefore, it is possible to implement more complex systems based on these circuits. A single-electron SRAM and a single-electron digital astrocyte system have already been proposed [28, 35]. In the following subsections both systems architectures will be shown and features such as area and power consumption will be displayed.

A. SRAM

Storage and recovery capabilities for large amounts of information are essential for most modern digital systems. Generally, in digital memories, storage bits are arranged in

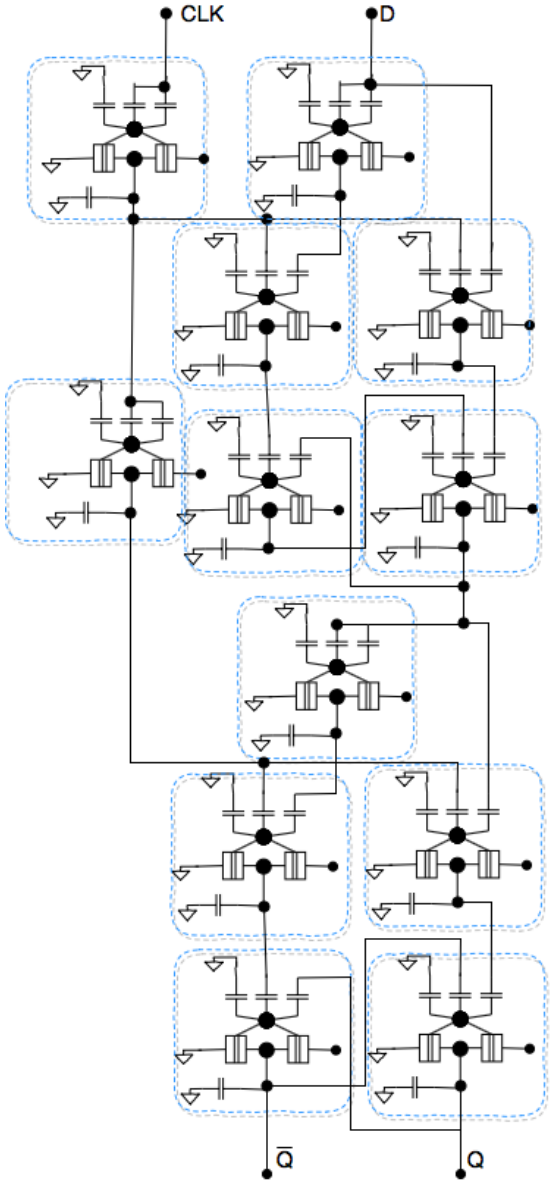

Fig. 9 SET D flip-flop positive edge-triggered circuit.

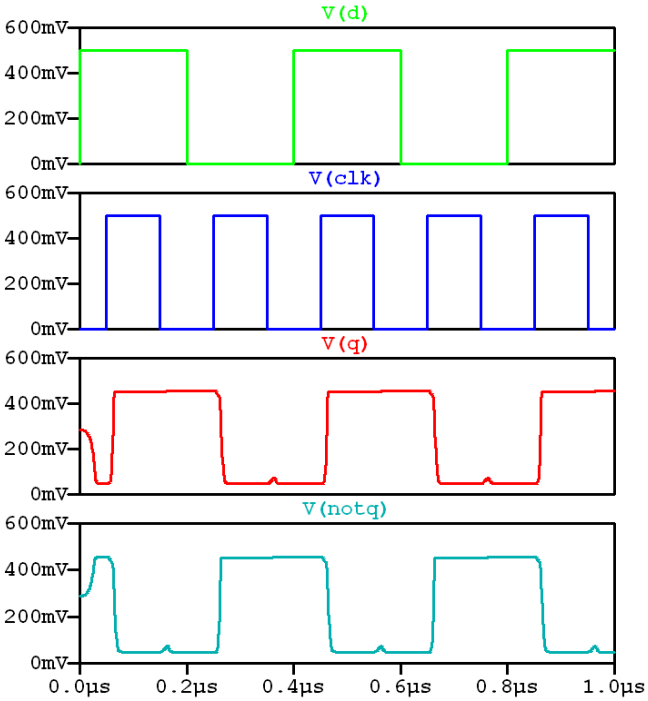

Fig. 10: Simulation results at room temperature for the SET D flip-flop positive edge-triggered circuit using arbitrary input signals [24].

two-dimensional arrays [36]. One of the most used digital memory in modern systems is the Random-Access Memory (RAM), which is a volatile read/write memory where the access time for reading and writing operations is independent of the data location in the memory array.

Specifically, in the static RAM (SRAM), the written data remains stored while there is power applied to the system. Thus, area and dissipated power are limiting factors in improving the performance of such memories [37]. Using nanoelectronic devices instead of CMOS transistors for implementing the SRAM could be one solution for those limitations.

The developed SET-SRAM system presented here can store 8 words of 8 bits and has separate controls for read and write addressing, allowing an individual and simultaneous execution of these operations (Fig. 11). The SET-SRAM cell consists of a D flip-flop, which can store 1 bit. These cells are arranged in an $8-bit$ array, creating a word. Each array consists of an $8-bit$ input, a clock and an asynchronous clear, besides read and write signals to indicate the current operation and independent select signals for each operation, which are used by the addressing logic as can be seen in Fig.12 [28].

To execute the read/write operation in the m_{th} word, both the corresponding operation signal and operation address should be selected in the m_{th} array. Because it is possible to realize a simultaneous read and write operation in the same array, an unstable situation could be reached in the output. To avoid this problem, both operations are also regulated by the system's clock. The write operation is executed during the rising of the clock signal, while the read operation is executed when the clock signal is low.

The SET-SRAM circuit was previously validated by simulation and the complete design has 1890 SET-NANDs [28]. It is worth mentioning that the area occupied by one SET-NAND can be estimated at approximately 172 nm^2 [28] and the SET-NAND power consumption, including static and dynamic dissipation, can be estimated in approximately 3.5 pW. The power consumption was estimated considering no offset charges. Table III presents values for area and power consumption for one SET-NAND, one SET-SRAM array (word), one SET-decoder, and the complete SET-SRAM considering operation at $1GHz$.

Table III. SET-SRAM area and power consumption

circuit	no. of NANDs	area	power
SET-NAND	1	172 nm^2	3.5 pW
array	206	35432 nm^2	721 pW
decoder	37	6363 nm^2	129.5 pW
SET-SRAM	1890	0.325μm^2	$6.6nW$

The whole 8x8 SET-SRAM system would occupy an area of 0.325 μm^2 and would consume 6.6 nW.

Table IV makes a comparison of power supply (V_{DD}), total area and average energy (E_{AVG}) computation among a SET-SRAM, a TFET-SRAM (tunnel field-effect transistor) and a CMOS-SRAM. The obtained results highlights the advantages of a nanoelectronic SRAM if compared to CMOS or TFET [38].

Hence, this SET approach solves area and energy consumption limitations faced by current applications. Moreover, the proposed architecture provides separate read and write addressing, allowing more versatile applications with lower latency time [28].

Table IV. Comparison among SET, TFET and CMOS 8x8 SRAMs

SRAM technology	V_{DD} (V)	E_{AVG} (fJ/access)	area (μm^2)
SET-NAND	0.5	≈ 0.302	0.325
3T-TFET [38]	0.45	1.64	6.91
6T-CMOS [38]	0.75	11	7.68

B. Digital astrocyte system

The hardware implementation of neural networks has been highly explored in the past decade. Such implementations are usually very computationally intensive, requiring powerful traditional hardware and often in large quantities. Therefore, a neuromorphic approach seeks to solve those issues [39]. Indeed, the CMOS-based neuromorphic implementation can be greatly optimized by replacing it with a nanoelectronic-based neuromorphic approach [5].

Recent experimental results show that astrocytes play a significant role in neural spike synchronization, synaptic transmission, and information processing [40]. The hardware implementation of astrocytes is the first step towards creating a fully neuron-astrocyte integrated neuromorphic circuit. Thus, the design of a digital SET-astrocyte system was developed [35]. This system is based on the 2D version of the spontaneous model of astrocytes [41].

Equations in that model describe the calcium (Ca^{2+}) oscillations in the astrocyte as a result of receiving an external stimulus, e. g., from a neuron. The spontaneous model has two major variables:

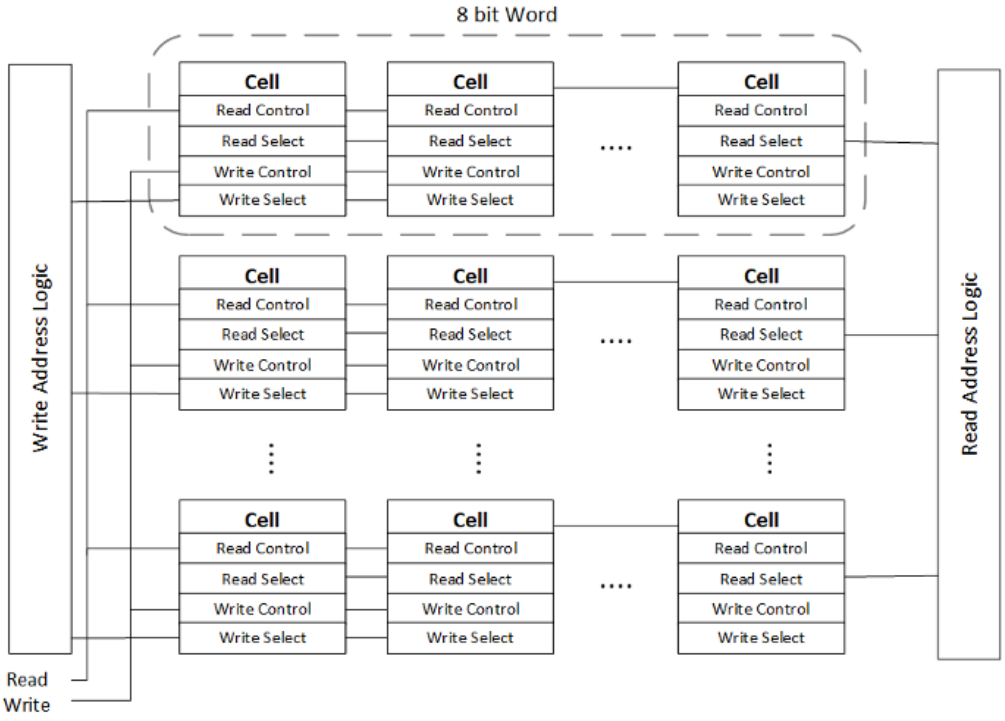

Fig. 11 Proposed SET-SRAM system [28]

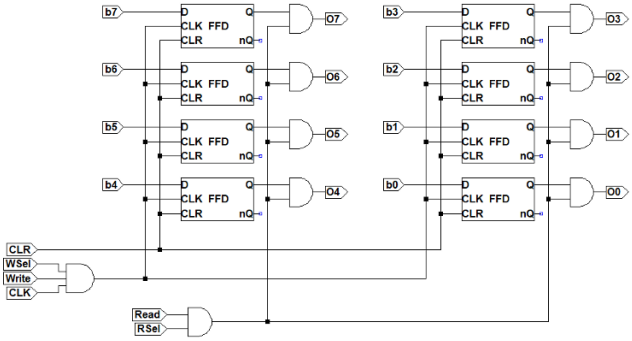

Fig. 12 SET-SRAM array [28].

- Ca^{2+} concentration in the cytosol (X); and
- Ca^{2+} concentration in the endoplasmic reticulum (Y).

Different levels of stimulus are stored in the V_{in} variable. There are also two main nonlinear terms used to build the circuit: V_{SERCA}, responsible for the $SERCA$ pumps, and V_{CC}. The parametric discretized equations can be seen in Haghiri *et al.* [41]. The original equations consider using 41 bits to avoid losing information. However, through exhaustive tests, it was determined that assigning 6 bits for the integer part and 14 bits for the decimal part provides good accuracy. Therefore, this implementation uses only 20 bits. Fig. 13 shows the complete SET-astrocyte system. The whole system is based on the SET-NAND gate. Values for V_{in}, $X[i]$, and $Y[i]$ are stored in the SET-SRAM proposed in the previous section.

The astrocyte control unit (ACU) provides the values of V_{SERCA} and V_{CC} by comparing $X[i]$ value to the conditions of the piecewise linear equations given in Haghiri *et al.* [41]. These values are forwarded to the pipeline (PiP) unit along with V_{in} value. Then, the PiP unit generates the next values for X and Y. In the sequence, values are stored at the output provider unit (OPU), which consists of two SET-SRAM modules. Finally, the OPU feeds the ACU to generate the next values of X and Y and providing the generated values to a DAC so that the values can be read in the output. At the end, the entire SET-astrocyte system has approximately 60000 SET-NANDs, occupying a total area of 10.32 μm^2 and consuming 210 nW. Those values, as the ones obtained for the SET-RAM, also reinforce the benefits of designing a nanoelectronic neuromorphic astrocyte system. The Ca^{2+} oscillation was obtained with fewer bits than previous works while still presenting a reliable output.

VII. Conclusion

In this paper a simple design flowchart for SETs was proposed taking into account the operating temperature and applied voltages. Based on this flowchart, digital circuits and systems were designed and implemented by simulation. The proposed design methodology used a SET-NAND gate as a building block for obtaining all other logic gates from it, employing the property of functional completeness. Despite the various available SET-NAND gates, the one used here was chosen because it has already been shown that it is prone to connectivity and works at room temperature. Also, a preliminary noise margin study of this SET-NAND gate showed that margins obtained here, even considering imperfections like background charges, are larger than the margins of CMOS technology, which is an interesting advantage of this type of circuit. Furthermore, simulation results showed that the SET-NAND gate is robust to background charges variations. Combinational and sequential circuits have been successfully implemented using the proposed methodology.

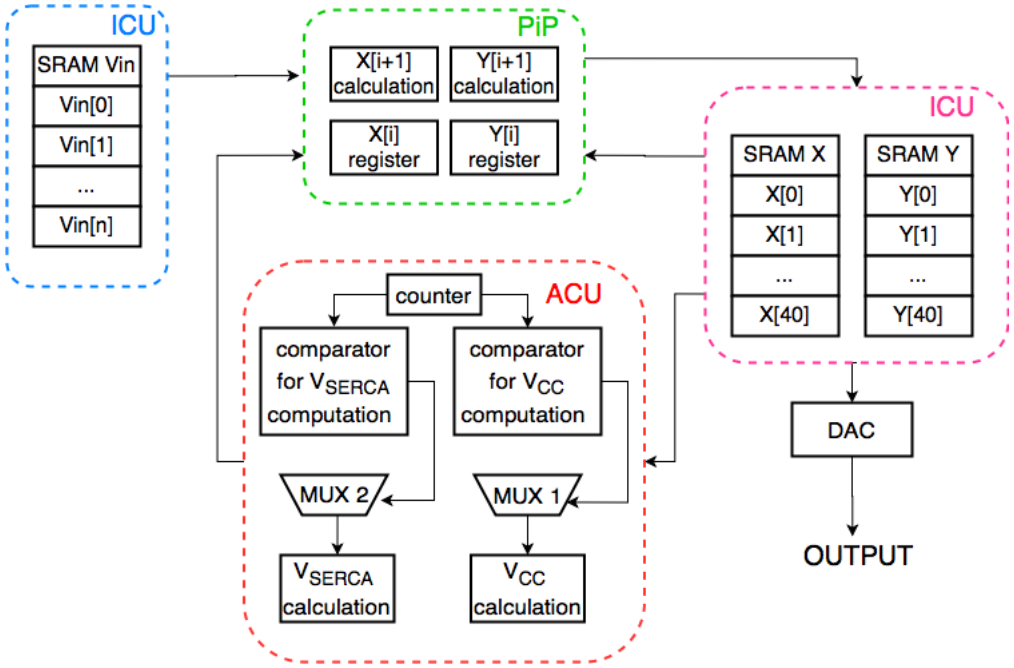

Fig. 13 Digital astrocyte block diagram [41]

In the end, two complex systems already implemented using the proposed methodology were presented: an SRAM and an astrocyte system. Both implementations, in addition to satisfactory results, showed the performance potential of large-scale circuits and systems based on SET in terms of robustness, area, and power consumption.

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